Docket Number: 10004086-1 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Ronald Kaneshiro et al.	:	Confirmation No.:	9456
Serial No.:	10/056,099	:	Art Unit:	2874
Filed:	1/22/2002	:	Examiner:	Daniel J. Petkovsek
For:	PASSIVELY ALIGNED FIBER OPTICAL ENGINE FOR PARALLEL OPTICS INTERCONNECT DEVICES	:		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 CFR §1.131

Sir:

Mikio Ishimaru declares that he is a patent attorney of the firm of The Law Offices of Mikio Ishimaru and a member of the State Bar of California; that he personally prepared the above-identified patent application; that prior to the November 2, 2001, filing date of the Boudreau U.S. Patent 6,574,399, entitled "Ceramic Waferboard for Integration of Optical/Optoelectronic/Electronic Components", he received the disclosure (see Appendix A) of the above-identified application from the Assignee; that on December 7, 2001, he sent an email to the inventors regarding a draft of the above-identified application; that on December 11, 2001, he received a marked up copy of the above-identified application; that on December 19, 2001, he sent the final documents to the inventors for signature; that on January 8, 2002, he received the signed documents back from two of the three inventors and learned that one of the inventors had left the employ of the Assignee; that on January 16, 2001, the third inventor was located and the final documents mailed to the third inventor; and that he received the signed final documents and caused the above-identified application to be mailed by U.S. Express Mail to the U.S. Patent and Trademark Office on January 22, 2001.

He further declares that all statements made herein of his own knowledge are true and that all the statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issuing thereon.

Respectfully submitted,

Mikio Ishimaru
Reg. No. 27,449
October 31, 2003

APPENDIX A

DESCRIPTION OF THE INVENTION

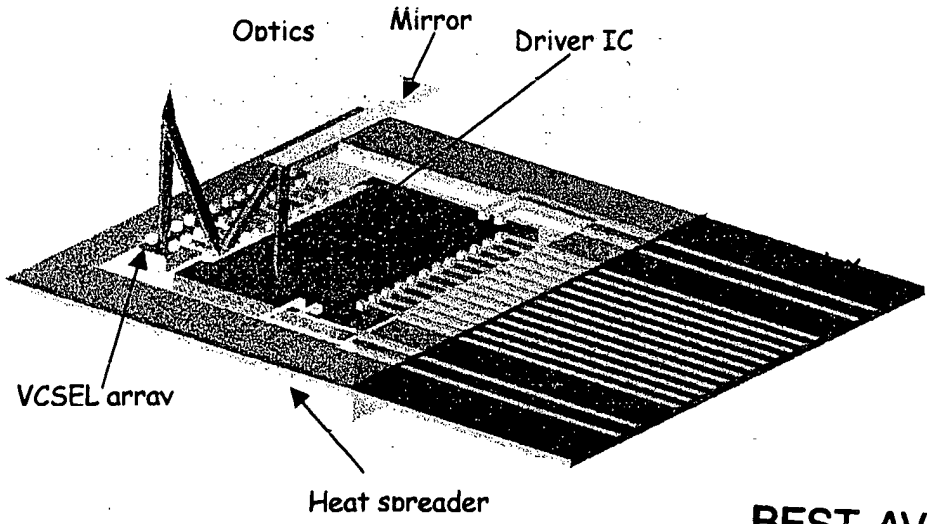
Conceptual design for a very fast fiber optical engine which can be manufactured using commercially available material, equipment and high volume production processes. Alignment of the optical components of this engine can be achieved ***passively***.

1. Passively aligned fiber Optical Engine (FOE) for parallel optics interconnect devices

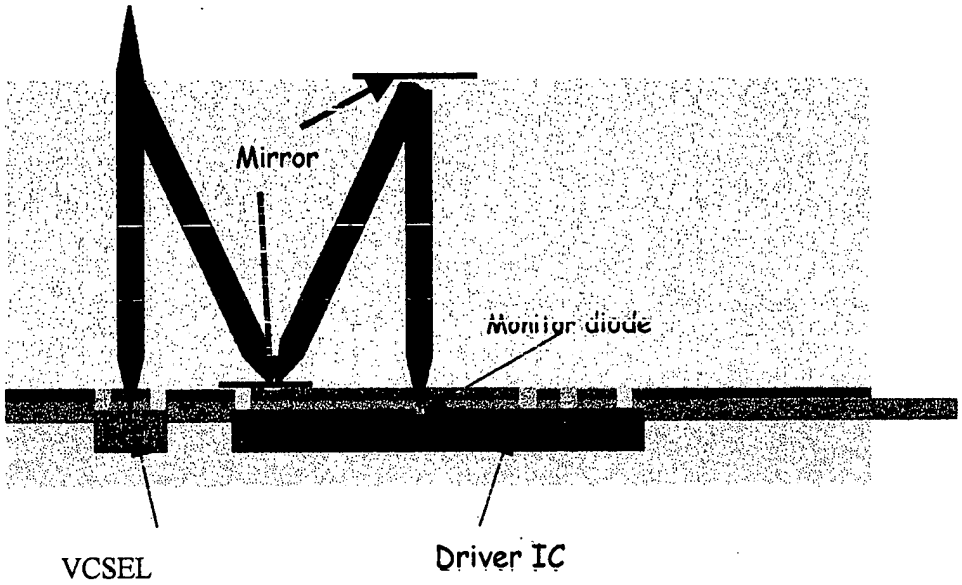
The concept of a 12 channel parallel FOE is graphically described in the picture below. The various components of the fiber optical engine are :

i. Vertical-cavity surface-emitting laser array (VCSEL)
ii. Optical substrate
iii. Driver integrated circuit (IC) with integrated feedback monitor
iv. Flex interconnection

Fiber Optical Engine



Cross section view



The driver IC continuously adjusts the light output of each individual channel of the VCSEL array through an integrated monitor diode array . The use of mirror on the optical substrate facilitates the signal feedback by re-directing the partial light beam from the VCSEL onto the monitor diode.

2. Components of the optical engine

2a. Optical substrate :

The substrate is made of optically clear material such as glass or molded polymer . Several functional features are incorporated onto the substrate.

- Optics (lens and mirror) to process the light output from the VCSEL array
- Metal traces for interconnecting the active chips to the outside
- Micro solder bump for self aligning the VCSEL and driver IC chip

Details of those functional features are shown on figure 3 and 4 on the next page.

Figure 3

Optical substrate - Front side

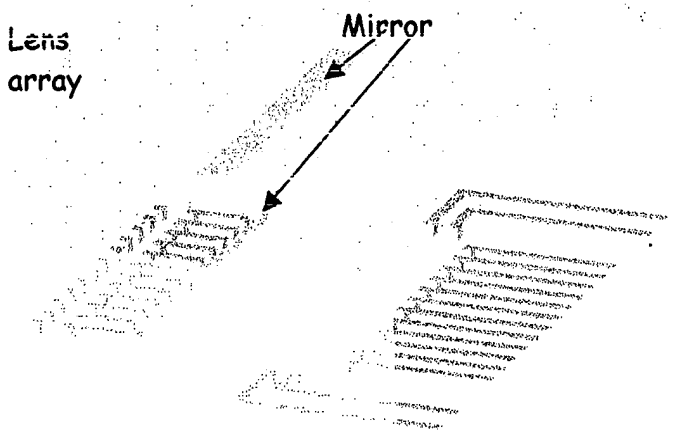
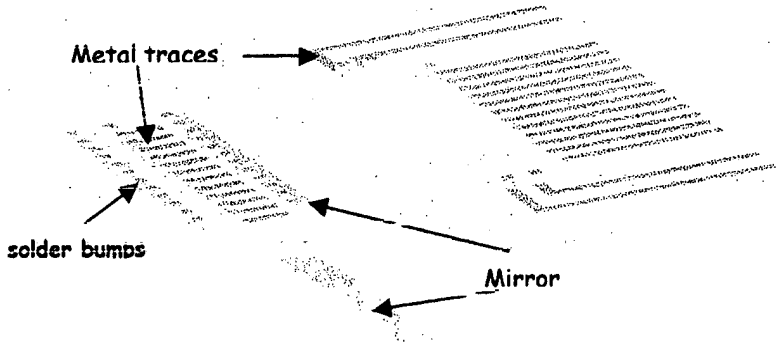


Figure 4



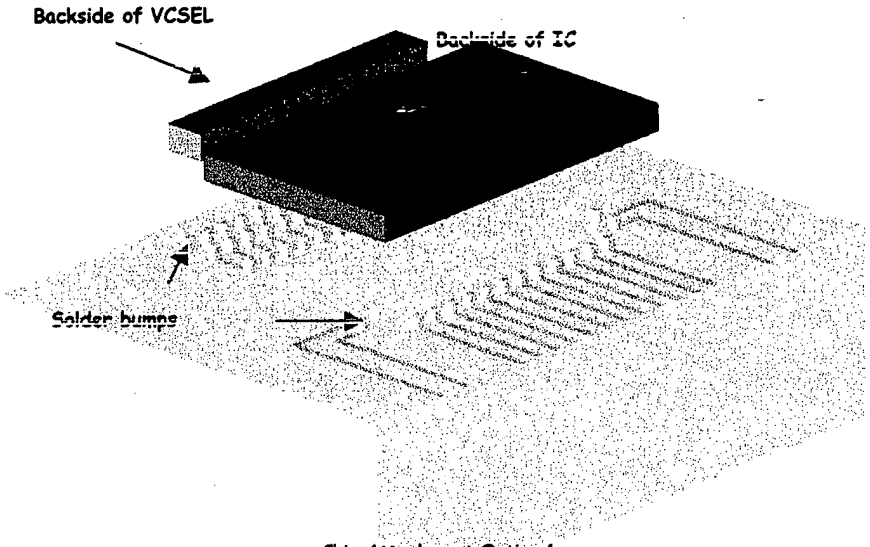
Optical substrate - backside

2b. VCSEL array and driver IC

The VCSEL array and the driver IC are passively aligned to the optical features on the substrate by three possible bonding techniques..

Chip bonding option 1

A thin layer of flux is applied to the optical substrate . The bonding pads of the VCSEL and driver IC are visually flip upside down and aligned to the micro solder bumps . The tackiness of the flux insures that the chips are adhered to the solder bumps. Very accurate alignment of the chip bonding pads to the solder bumps is not necessary at this stage of the process.. The work piece is put through an IR oven in which the solder bumps are brought up to a temperature above its melting point. The surface tension of the molten solder pulls the chips back into alignment with the substrate.

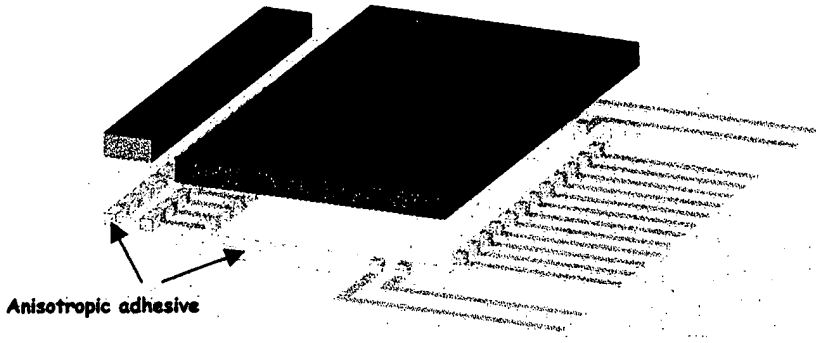


Chip Attachment Option 1
self alignment of eutectic solder bumps

CHIP BONDING OPTION 2 :

This method relies on another conventional method which is popular with the manufacturing of flat panel displays . A layer of anisotropically conductive adhesive (ACA) is stenciled on the substrate. An alternate way is to punch a frame preform out of the ACA material supplied in film format. The curing of the adhesive can be accomplished through exposure to heat or UV light depending on the specific types of materials. UV light curing is preferred in this application as the room temperature curing is expected to introduce less optical misalignment than the heat curing method due to the thermal expansion coefficient of the chips and optical substrate.

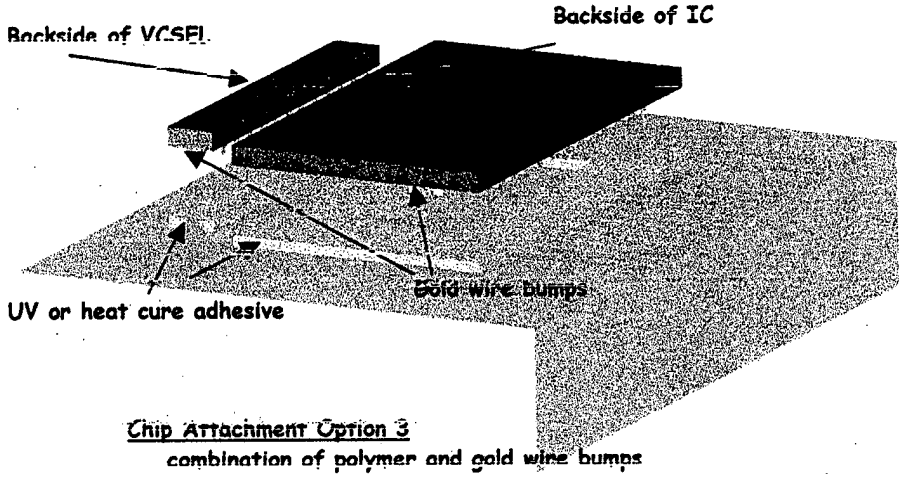
A precision die bonder picks up the chip and aligned it to the substrate via fiducials which are put on the surface of the chip as well as the substrate. A load is applied between the chip and the substrate while the ACA is cured by localized heat or UV light.



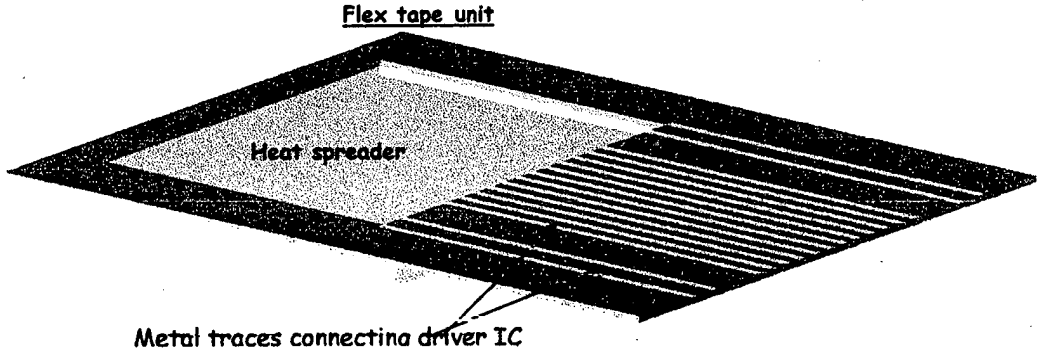
Chip Attachment Option 2
combination of polymer and gold bumps

CHIP BONDING OPTION 3 :

Gold wire bumps are formed on the bonding pads of the chip surface : the tail wire from a ball bond is cut and flattened to form the gold wire bump. An UV or heat cure adhesive layer is applied to the optical substrate . The chip is flip chip attached and held under load onto the substrate. Alignment of the chips to the substrate is accomplished via fiducials on the surface of the chip and substrate. The curing of the adhesive takes place while the pieces are held together. The shrinkage of the adhesive upon curing forces the gold bumps to make contact with the metal traces on the optical substrate.

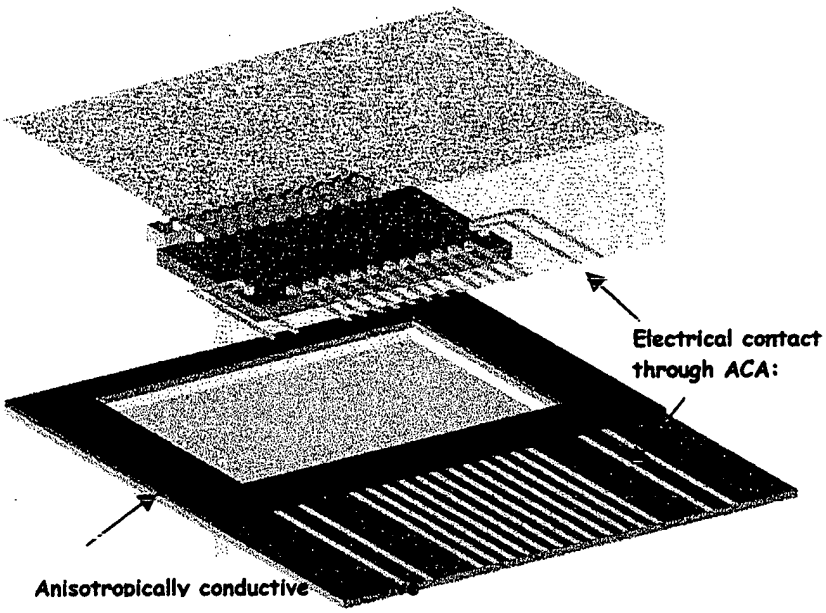


2c. Flex tape connection



AN ANISOTROPICALLY CONDUCTIVE ADHESIVE IS STENCILED ON THE FLEX TAPE UNIT . METAL TRACES ON THE OPTICAL SUBSTRATE SUBASSEMBLY IS ALIGNED TO THOSE ON THE FLEX TAPE.

The bonding of the optical subassembly and the flex tape unit is achieved through the curing of the anisotropically conductive adhesive.



ADVANTAGES OF THE INVENTION

1. ***Product performance***

   Shorter interconnections provided by micro solder bumps instead of bond wires : less parasitics for very high speed devices. Electromagnetic radiation is suppressed when the bond wires are not present.

2. ***Simplicity in manufacturing***

   The alignment of all key components (lens, VCSEL and monitor diode on IC) can be achieved passively.

   All equipment and materials used are commercially available. Assembly processes are widely used by other industries.

3. ***Wafer scale manufacturing approach for higher throughput***

   The assembly of the VCSEL arrays and driver integrated circuits can be done on a wafer size optical substrate.

4. ***Lower final product cost from pre-testability of FOE in wafer format***

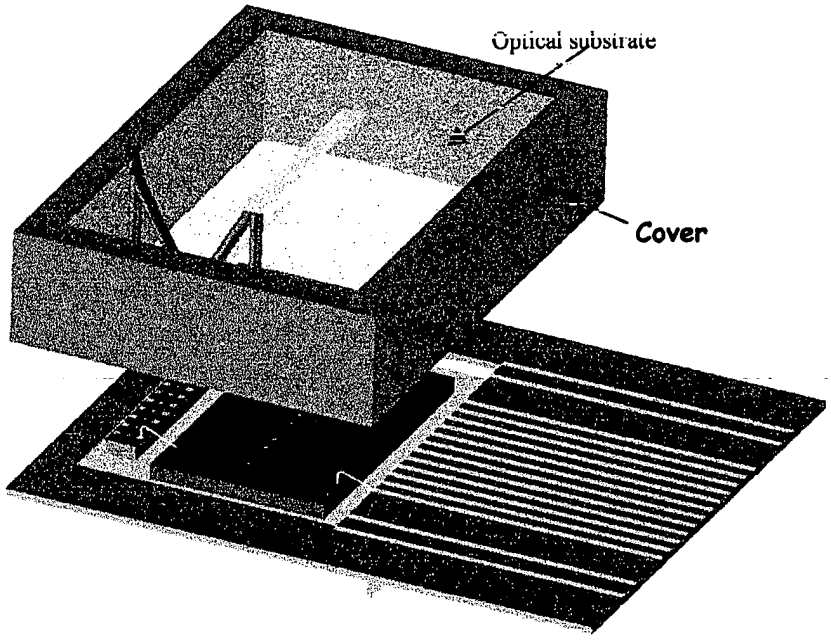
   Burn in of the fiber optical engine can take place in wafer format. Only good units will be used to manufacture the final fiber product.

CURRENT PRACTICE AND ITS DISADVANTAGES :

The VCSEL array and the driver IC are bonded to the flex unit first. Gold bond wires are used to make electrical connection between the chips and flex tape.

The optical substrate is bonded to a cover .

- VCSEL array as well as the monitor diodes on the driver IC must be aligned to the optical features on the substrate : **active alignment** of the VCSEL array to the lens must be used . Since the monitor diodes must also be aligned to the lens , the position of the driver IC with respect to that of the VCSEL array needs to be precisely kept with some effort.
- Wafer scale manufacturing is not possible
- Burn in of the FOE can only take place after the complete unit is assembled.
- The bond wire connection has a negative impact on the speed of the device. EMI control for very high speed device can be quite a challenge for this packaging method.



Tittle: Conceptual design for a very fast fiber optical engine which can be manufactured using commercially available materials, equipment and high volume production processes. The alignment of the ptical components of this engine can be achieved passively.

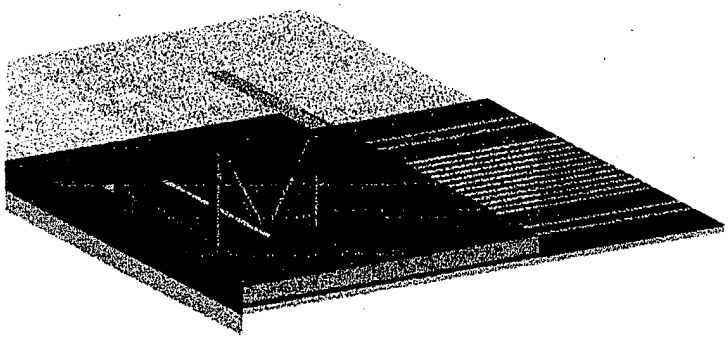
****

Amendment

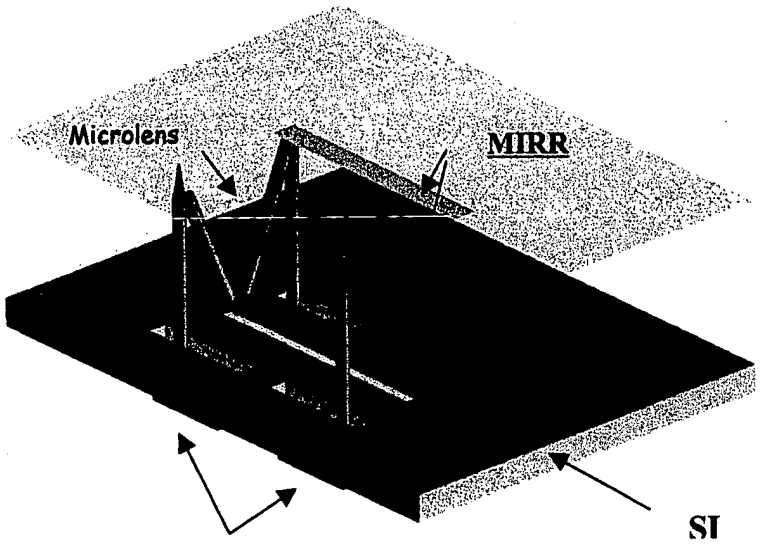
To demonstrate the flexibility and scalability of the optics engine concept, the following pictures describe the application of such a concept to making a 4+4 parallel optical transceiver module .

Instead of putting all active components (emitter, detector and driver integrated chip) on the optical substrate, an alternative option is to put all the components and their interconnect circuitry on a second substrate such as silicon. The use of a separate silicon substrate offers several advantages: benefits from existing silicon processing technologies such as multiple metal layers, incorporation of passives in the bulk of the silicon.

Application of the Optics Engine concept
in
a 4+4 parallel optical transceiver module

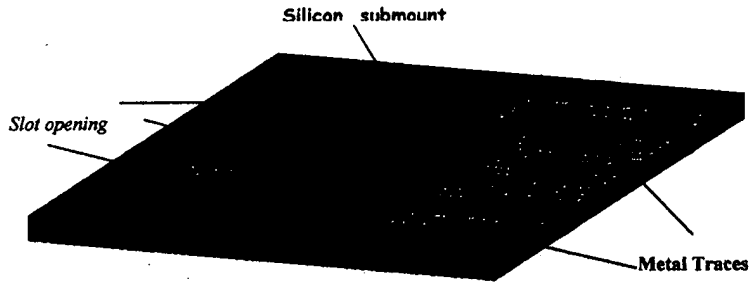


Optics engine sub-assembly for the 4+4 transceiver



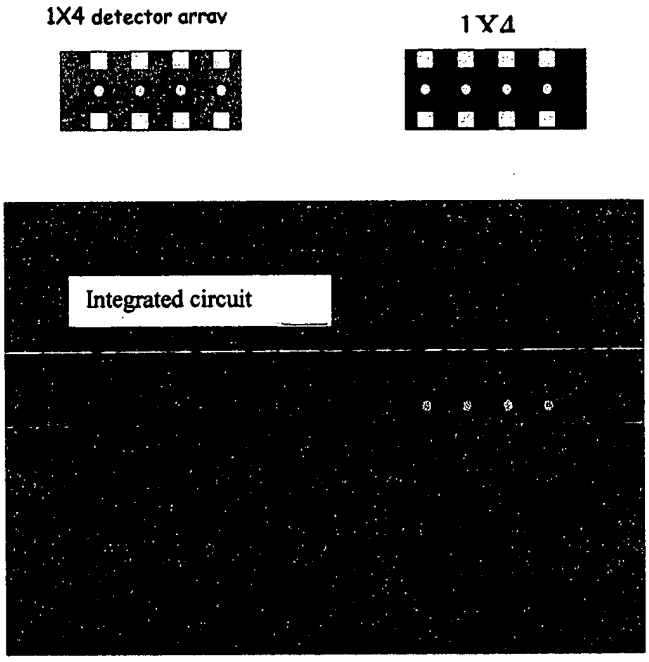
1X4 VCSEL AND 1X4

Construction of the engine sub-assembly

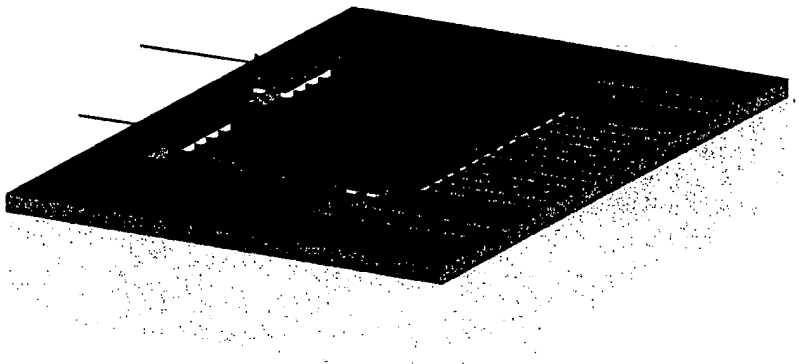


Lens substrate bonded /aligned to the Silicon submount

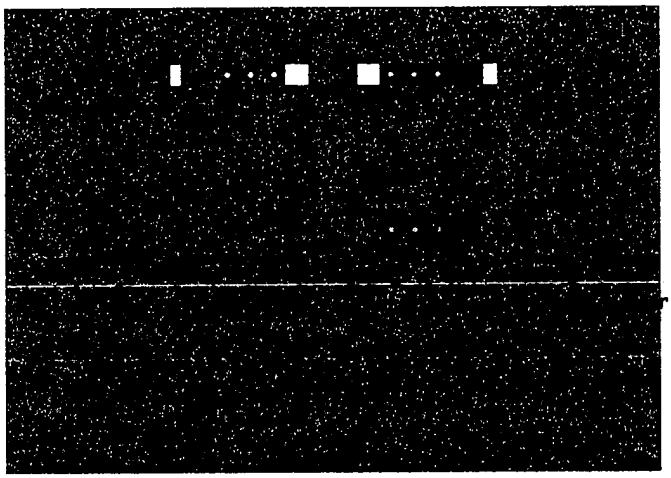
Active components of the 4+4 transceiver



Active components flip chip bonded to the silicon substrate



Actives components viewed through the openings on the silicon substrate



Cross section view